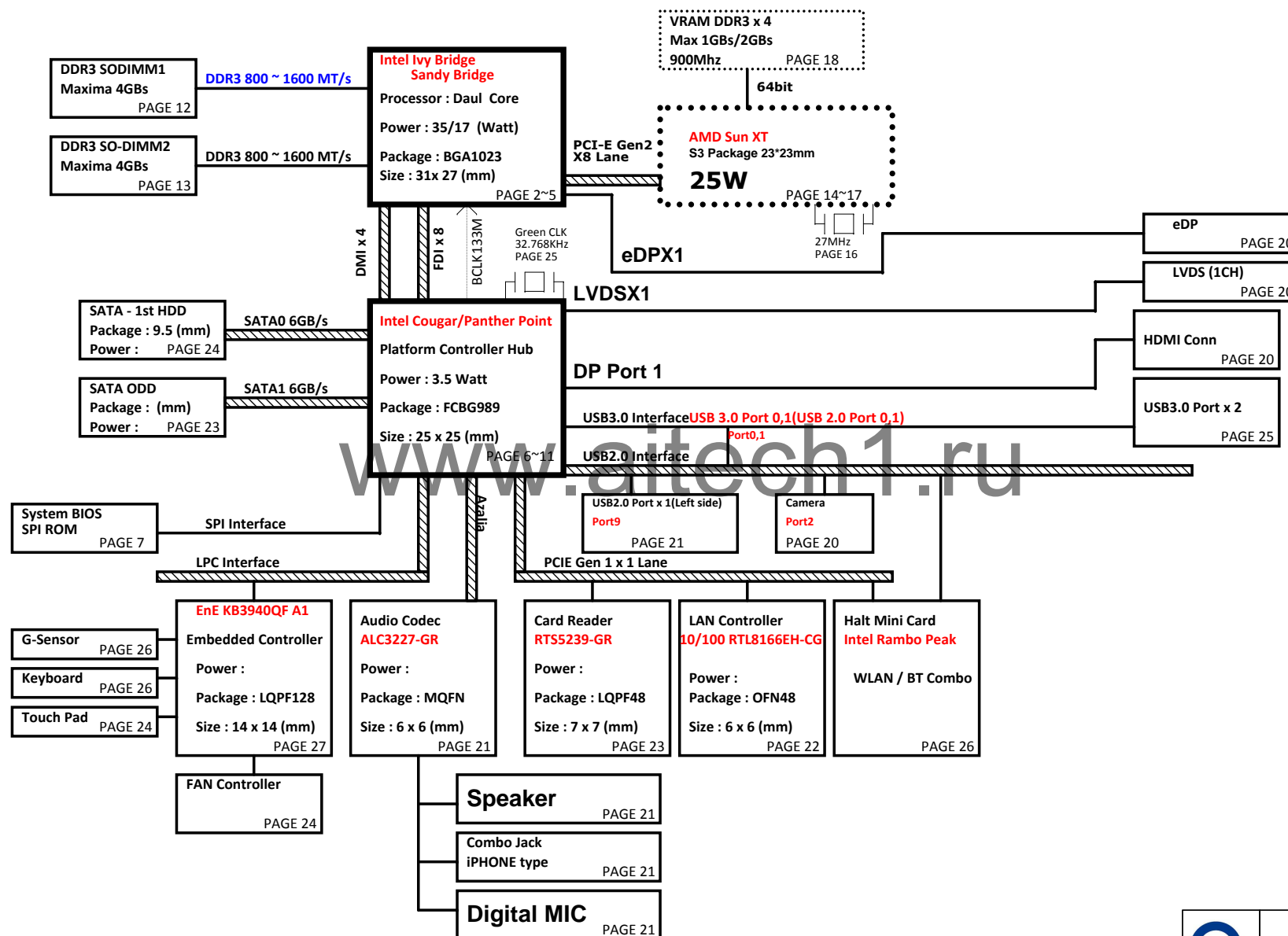


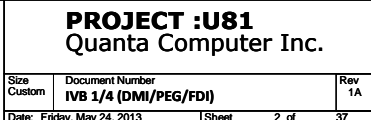
U81 DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram

PCB 6L STACK UP

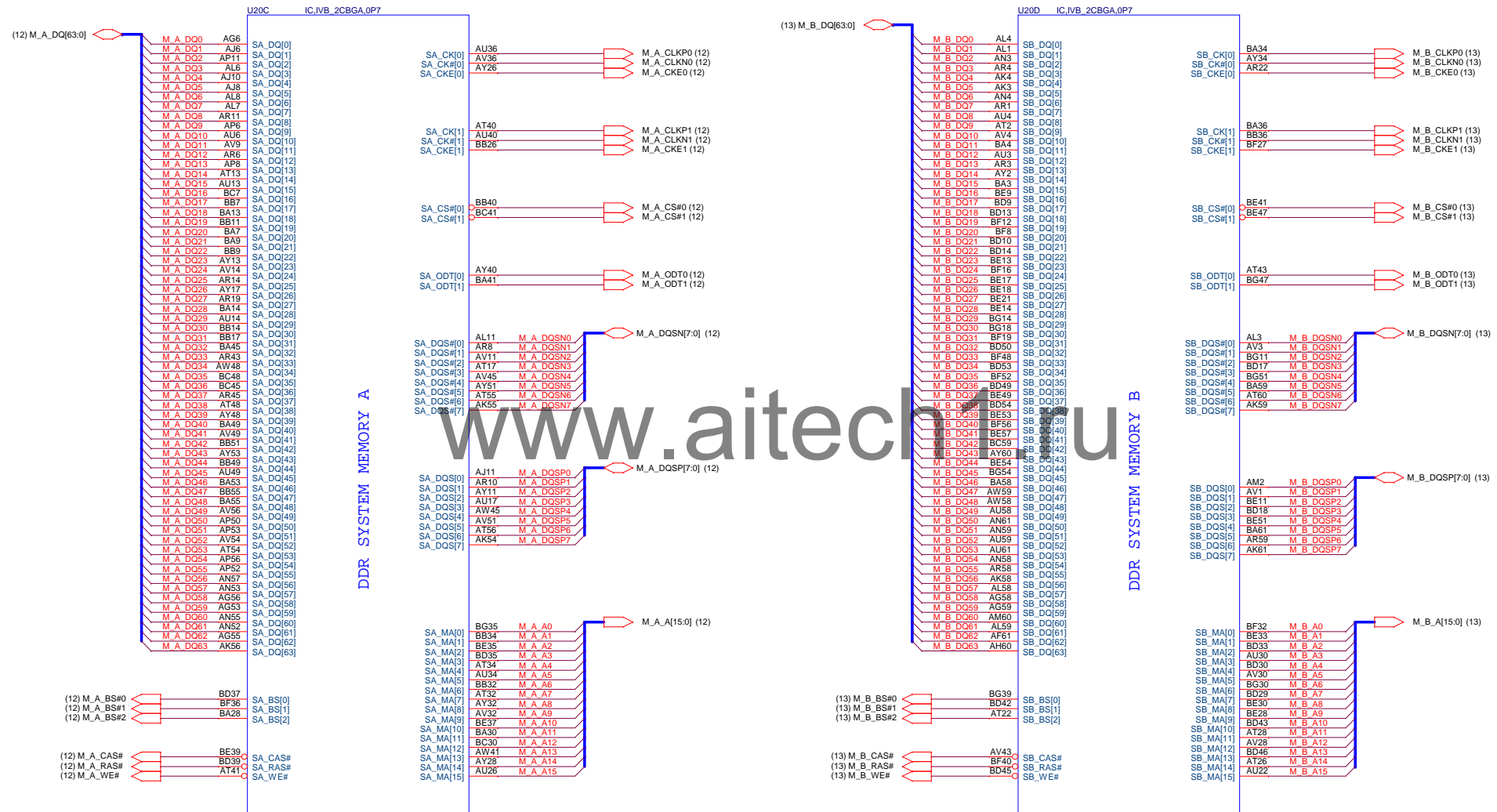
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

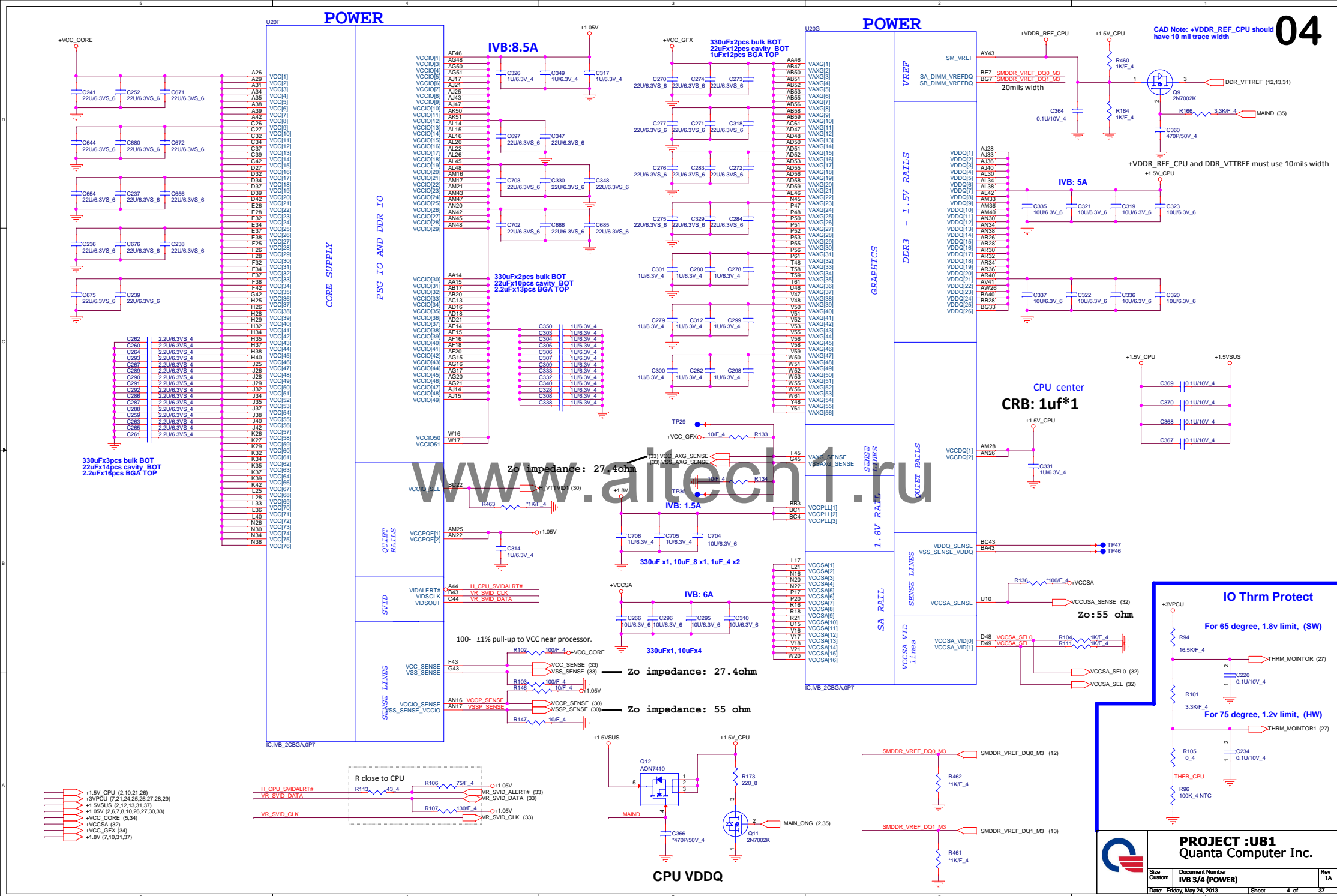


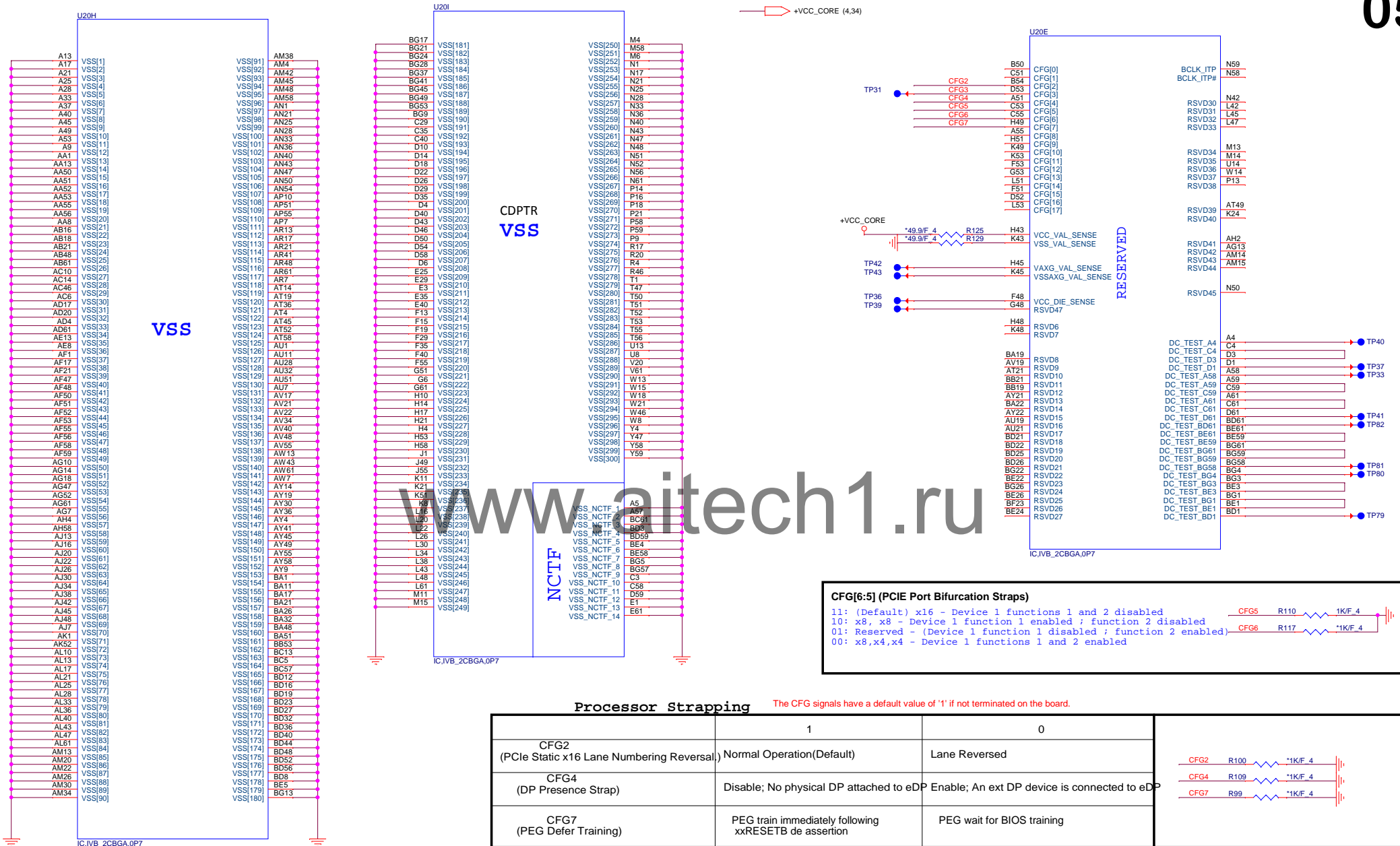
02



Ivy Bridge Processor (DDR3)







CFG[6:5] (PCIe Port Bifurcation Straps)

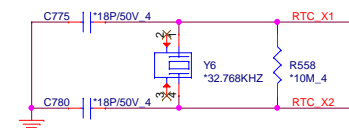
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

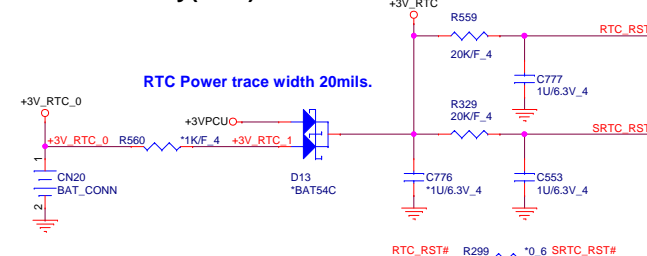


07

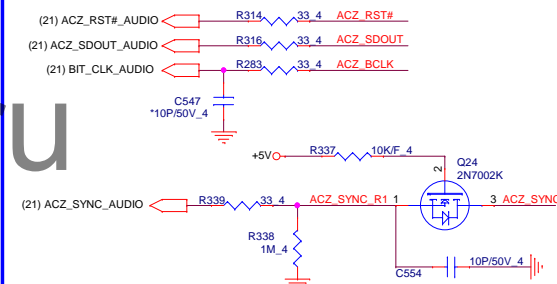


no stuff If use green Clock

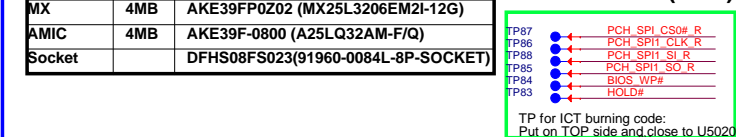
30mils



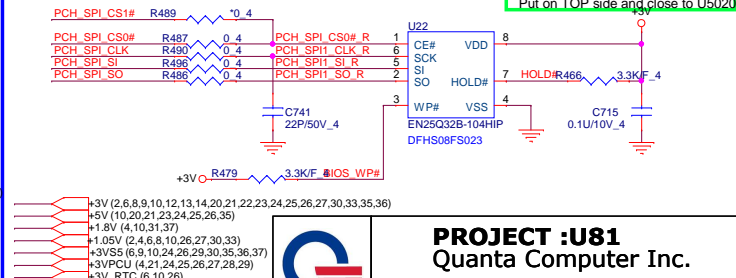
G)



PCH SPI ROM(CLG)



TP for ICT burning code:
Put on TOP side and close to U5020



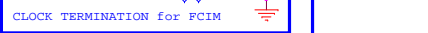
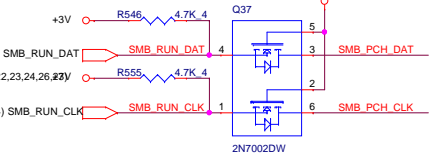
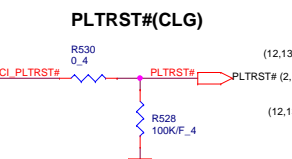
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
Date: Friday, May 24, 2013	Sheet	7 of 37

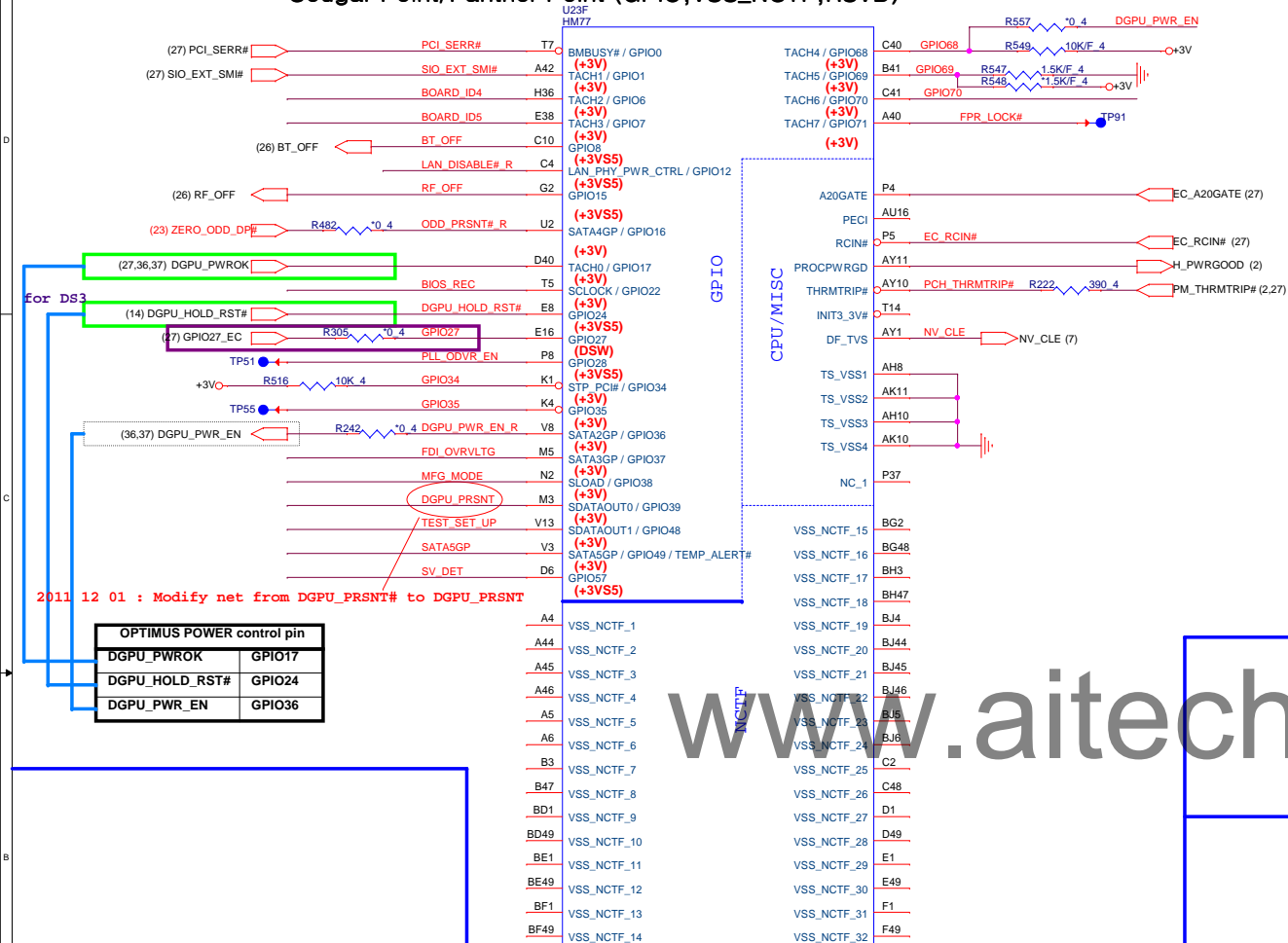
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td></td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI		1	LPC	
GNT1#	GNT0#	Boot Location											
1	0	SPI											
	1	LPC											
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ES1 strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

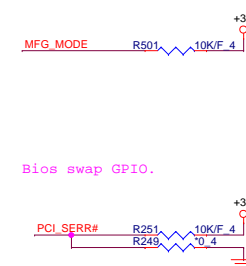


GPIO Pull-up/Pull-down(CLG)

for D53

+3V_DEEP_SUS

MFG-TEST



for D53

+3V_DEEP_SUS

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

BIOS RECOVERY

High = Disable (Default)

Low = Enable

SV_SET_UP

High = Strong (Default)

TEST DETECT

Low = Default

SATA2GP/GPIO36

Reserved only

FDI TERMINATION VOLTAGE OVERRIDE

Reserved only



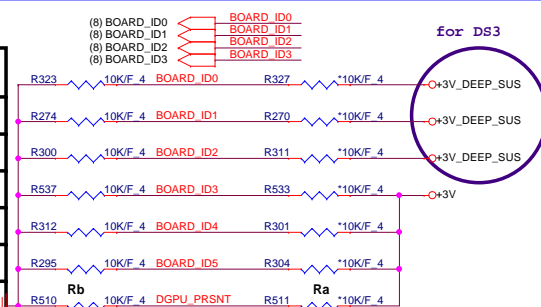
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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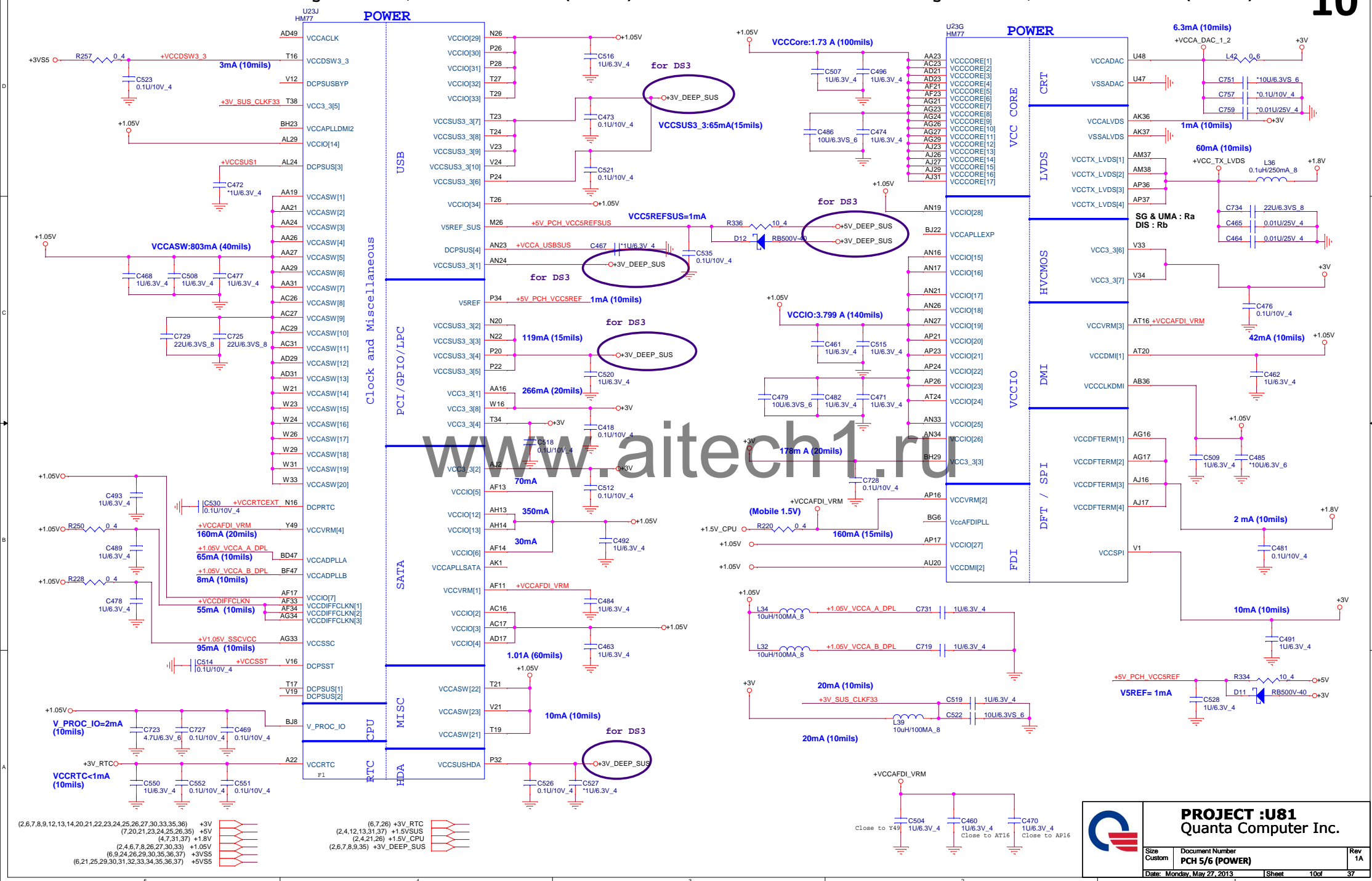
Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0 UMA: 0 DIS: 1
U81 UMA	0	0	0	0	0	0
U81 SWG	0	0	0	0	0	1
14"	0	0	0	0	0	0
15.6"	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

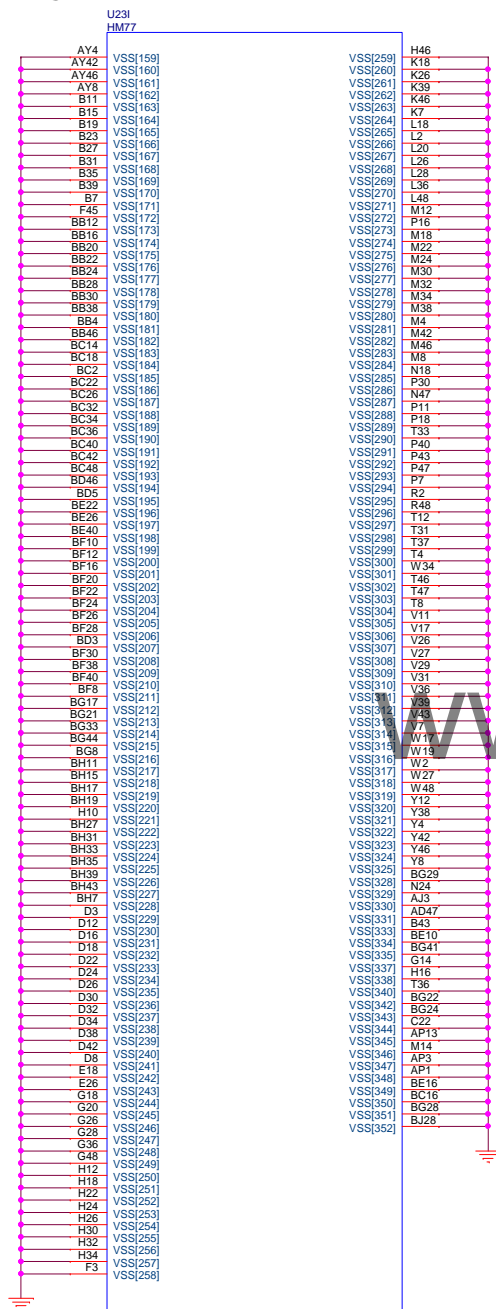


SG	UMA
Stuff	Ra Rb
NC	Rb Ra

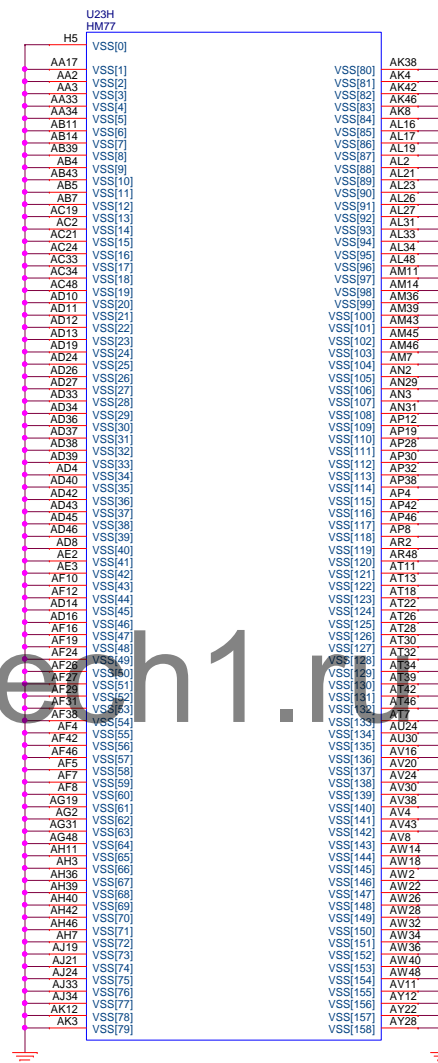
Cougar Point/Panther Point (POWER)

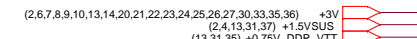


Cougar Point/Panther Point (GND)

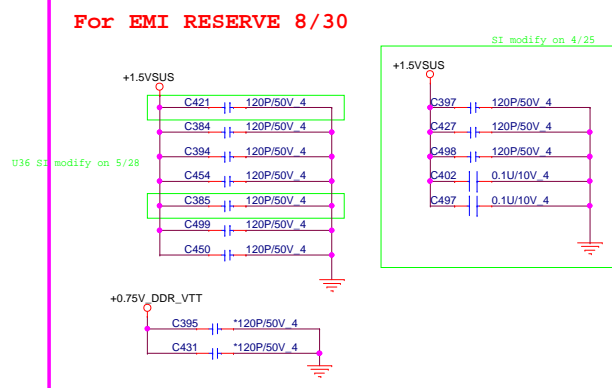


Cougar Point/Panther Point (GND)

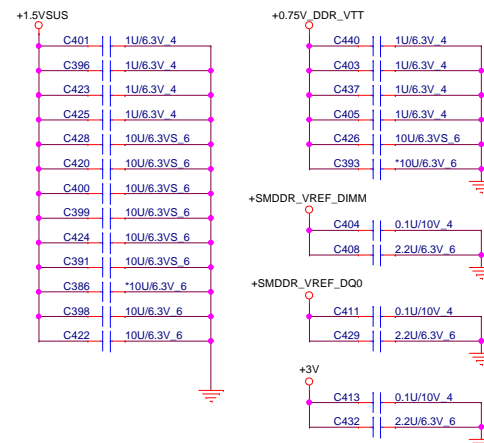




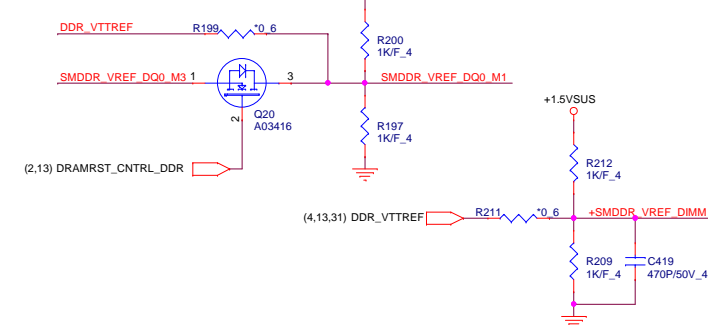
DQ53	174	M A DQ55
DQ54	176	M A DQ51
DQ55	181	M A DQ61
DQ56	183	M A DQ60
DQ57	191	M A DQ59
DQ58	193	M A DQ63
DQ59	195	M A DQ56
DQ60	180	M A DQ55
DQ61	182	M A DQ57



Place these Caps near So-Dimm0.



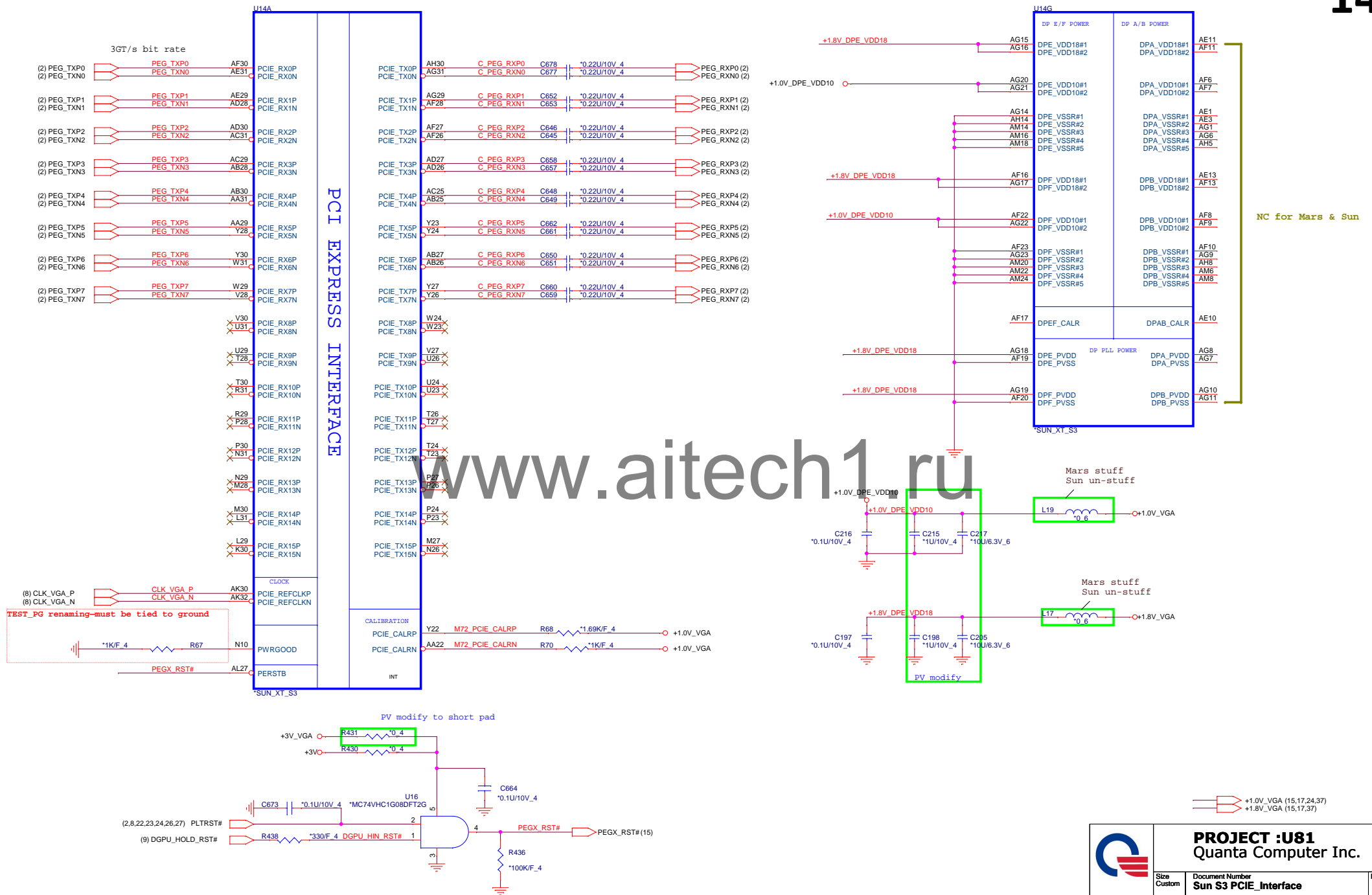
VREF DQ0 M1 Solution



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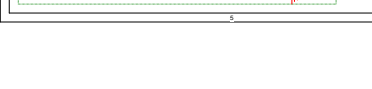
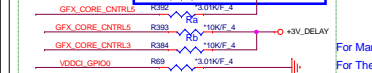
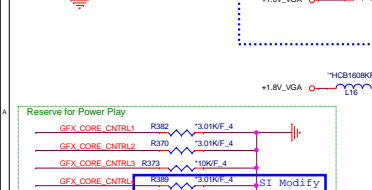
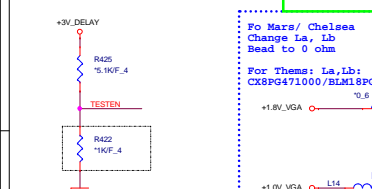
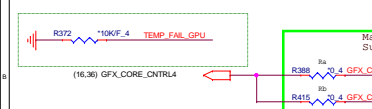
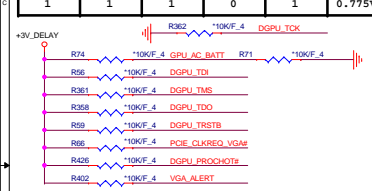
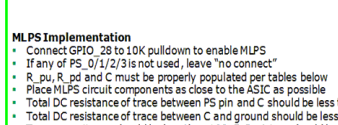
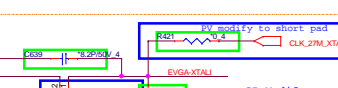
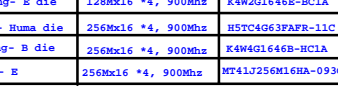
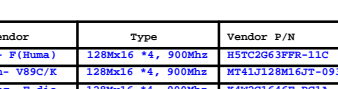
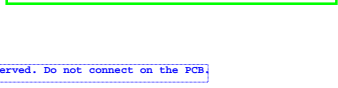
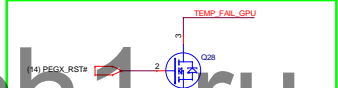
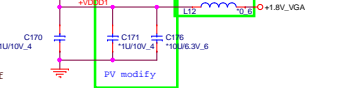
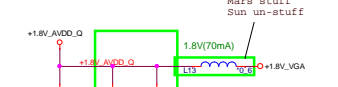
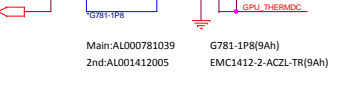
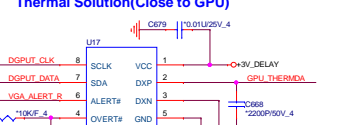
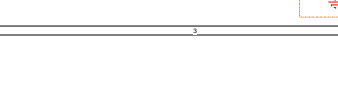
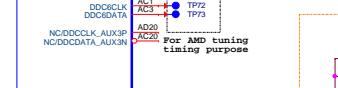
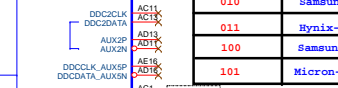
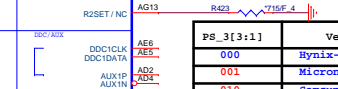
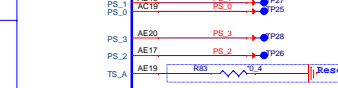
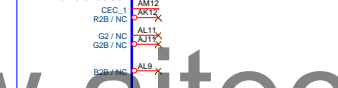
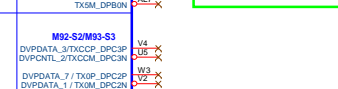
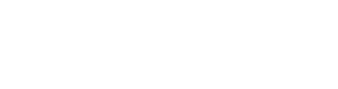
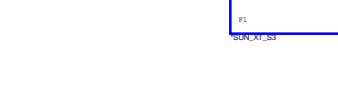
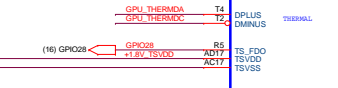
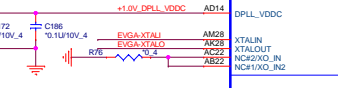
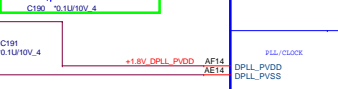
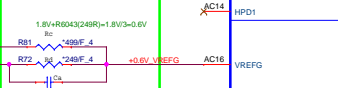
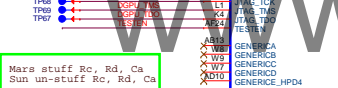
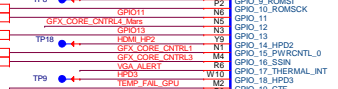
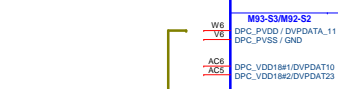
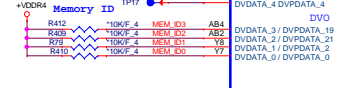
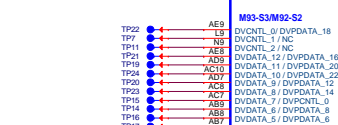
Size Custom	Document Number DDR3 DIMM0-STD(4.0H)	Rev 1A
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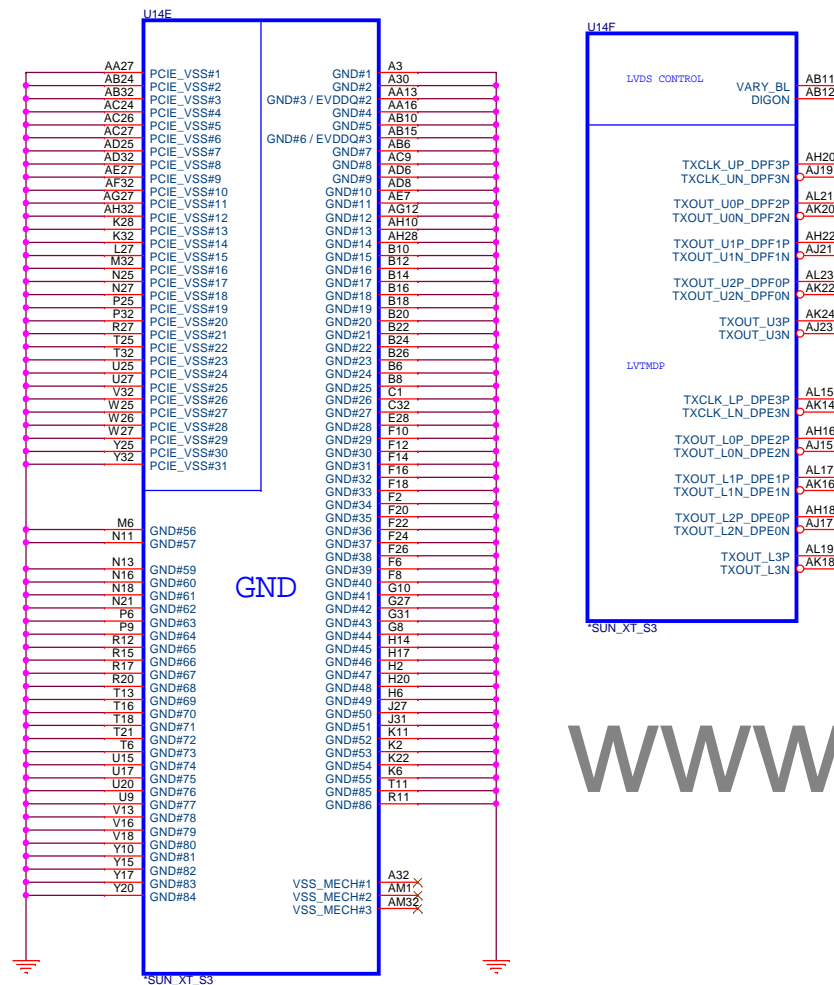




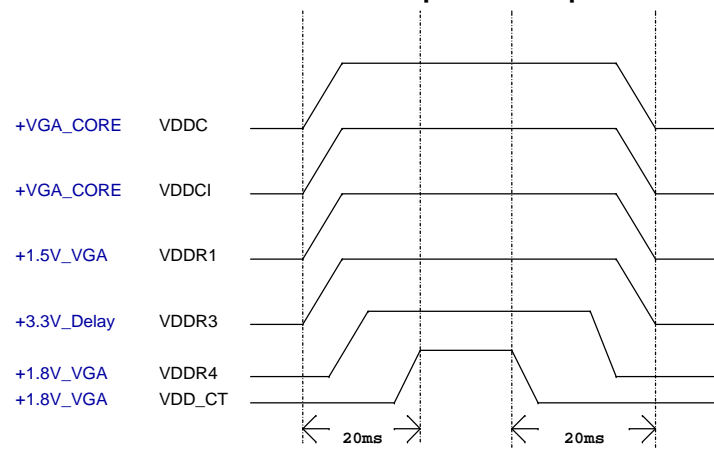
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	0	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	1	0	0.975V
1	0	1	1	1	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	1	0	0.775V

Default

Access to SMBus are SDA/SCL is mandatory on all designs
Add test points on SMBus and SDA/SCL for debugFor Mars: Stuff Ra only => VDDC 1.1V
For Thems: Stuff Ra, Rb => VDDC 1.0V



Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

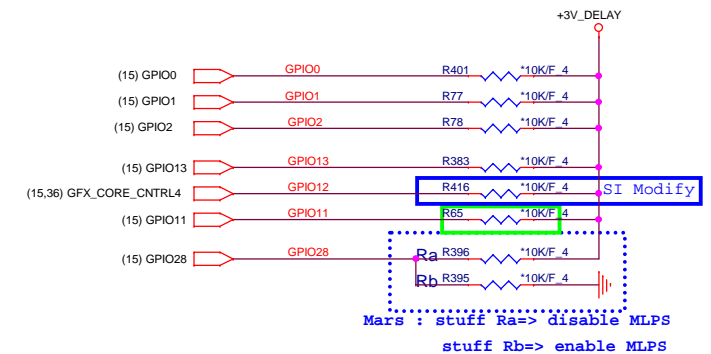
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 3K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

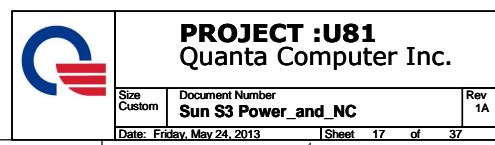
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

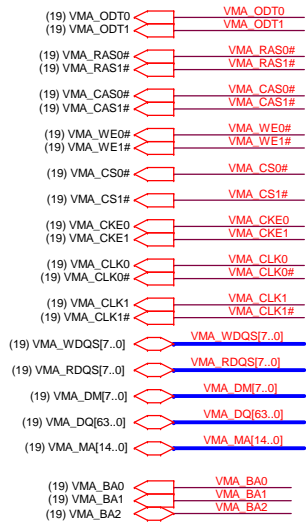
GPIO21 H2SYNC GENERICC GPIO8 GPIO2



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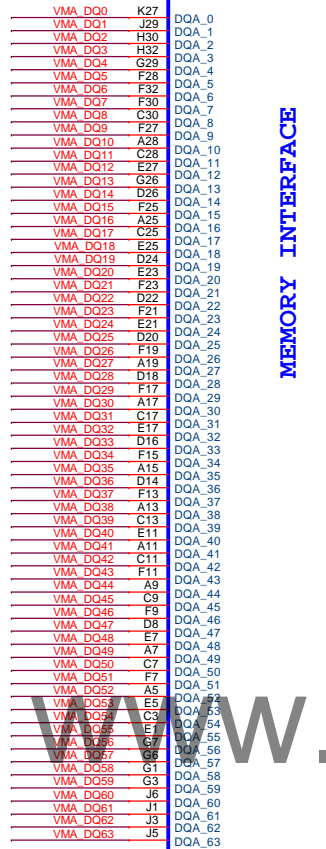
Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
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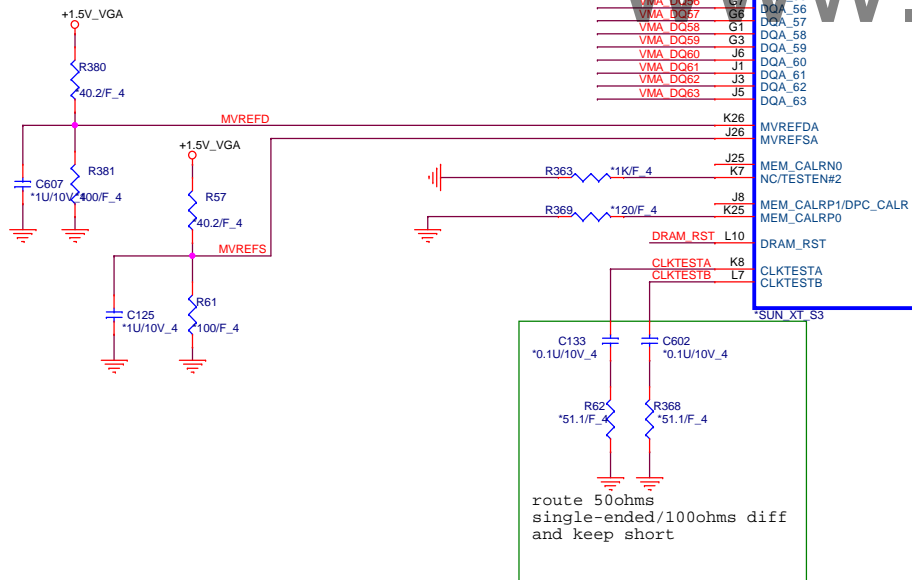
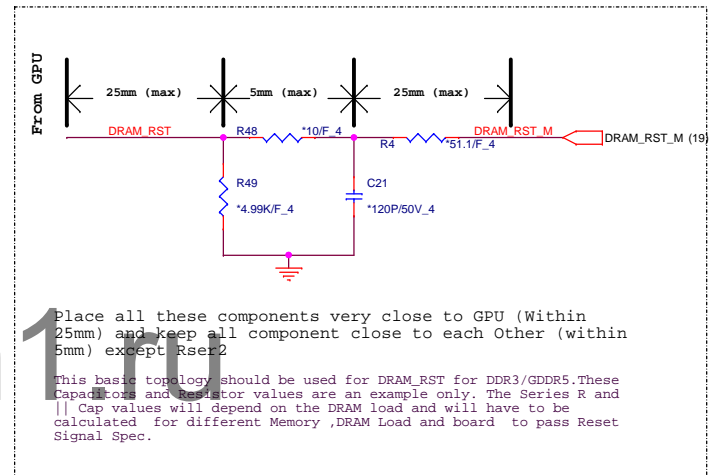
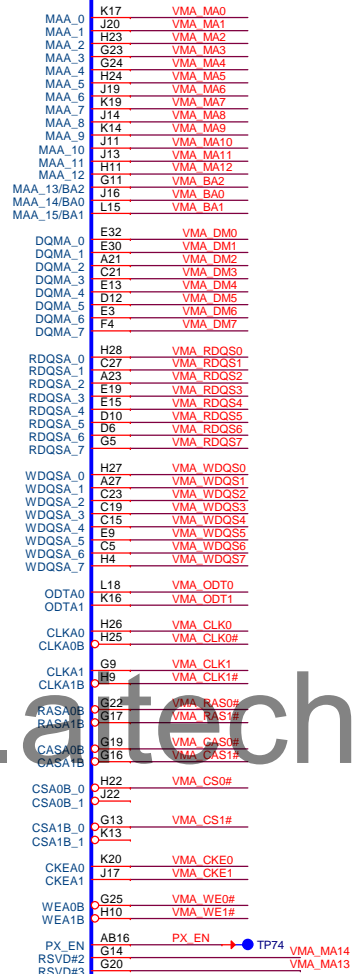


support 1gbt
 VRAM (64M X 16)

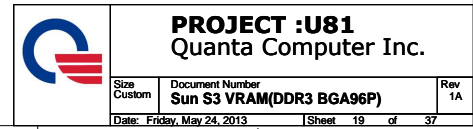
U14C



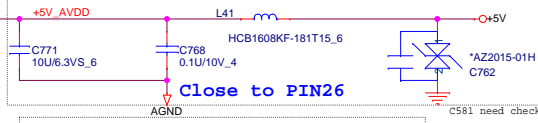
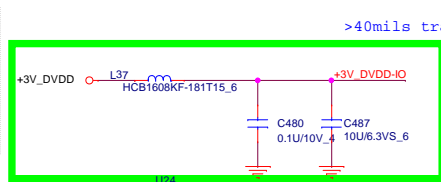
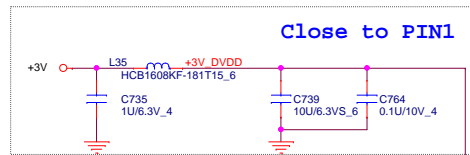
MEMORY INTERFACE



PROJECT :U81
 Quanta Computer Inc.

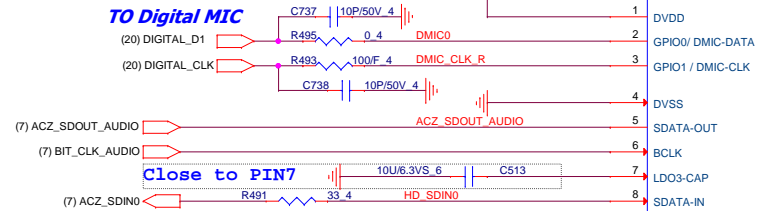


Close to PIN1

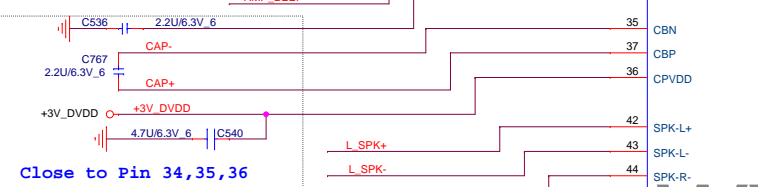
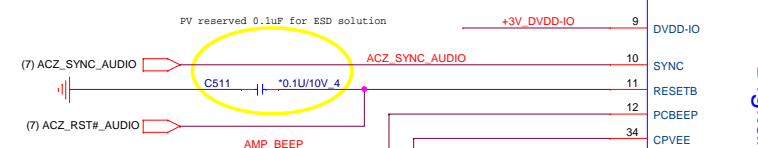


(7, 10, 20, 23, 24, 25, 26, 35) +5V
(2, 6, 7, 8, 9, 10, 12, 13, 14, 20, 22, 23, 24, 25, 26, 27, 30, 33, 35, 36) +3V
(2, 4, 10, 28) +1.5V_CPU

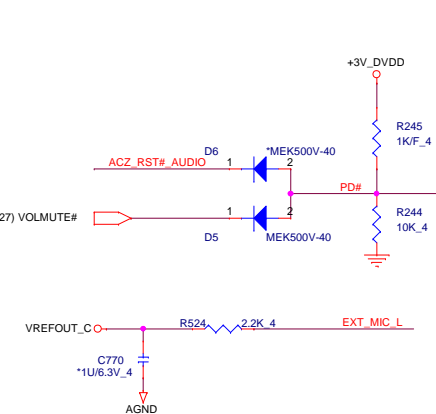
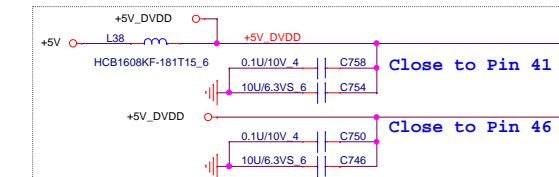
TO Digital MIC



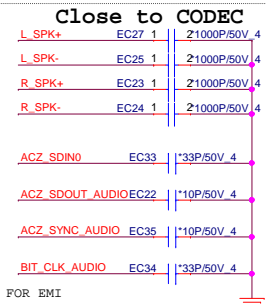
Close to PIN7



Close to Pin 34,35,36

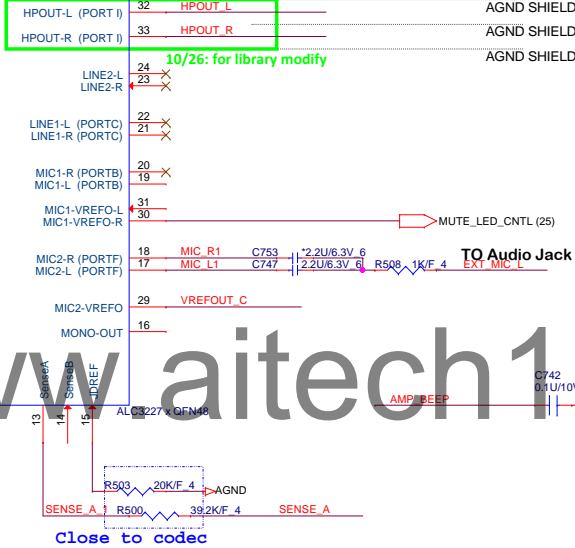


USB 2.0 AND AUDIO COMBO JACK



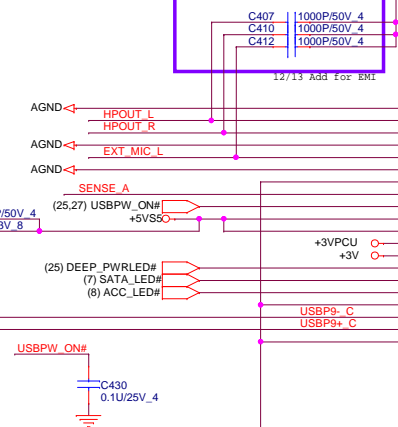
Analog

Digital



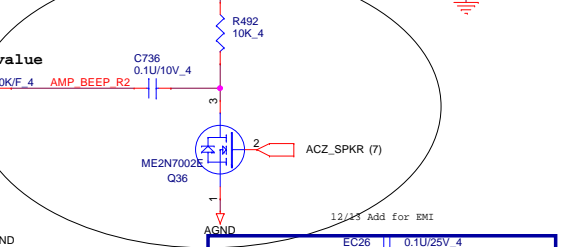
Close to codec

Check layout mount location

Close to Speaker
Speaker 4 ohm: 40mils

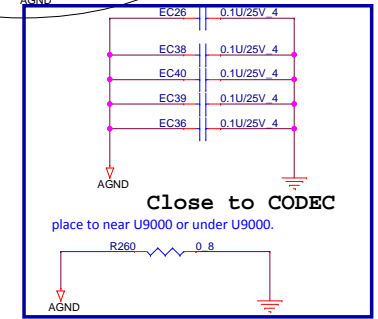
TO Headphone jack

TO Internal Speakers



Close to CODEC

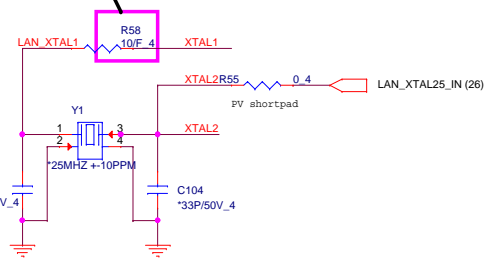
place to near U9000 or under U9000.



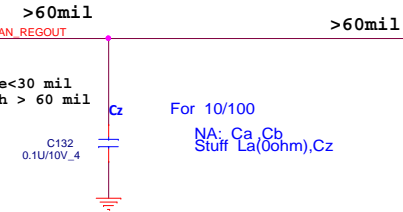
PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC 3227/D-MIC	1A
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For EMI 0 ~ 22 ohm

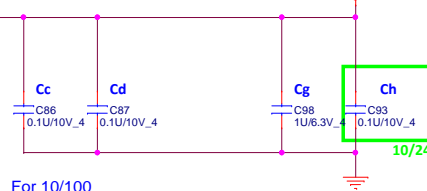


Power trace Layout 宽度 > 60mil



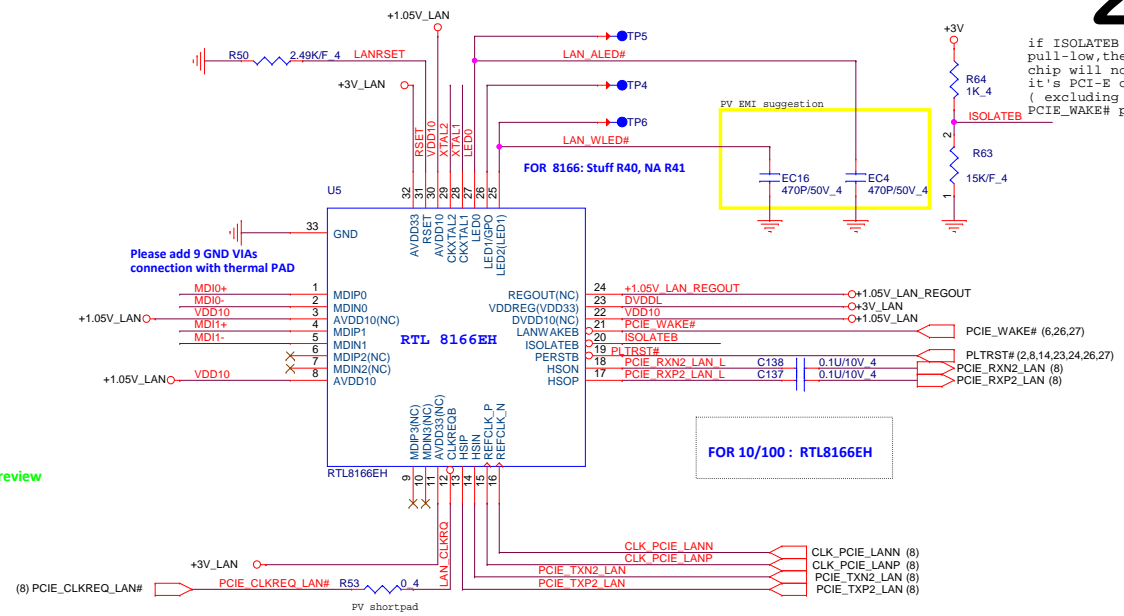
For 10/100

Place Cc,Cd close to each VDD10 pin-- 8, 30



For 10/100

Place Cg Ch close to each VDD10 pin-- 30 (reserve)

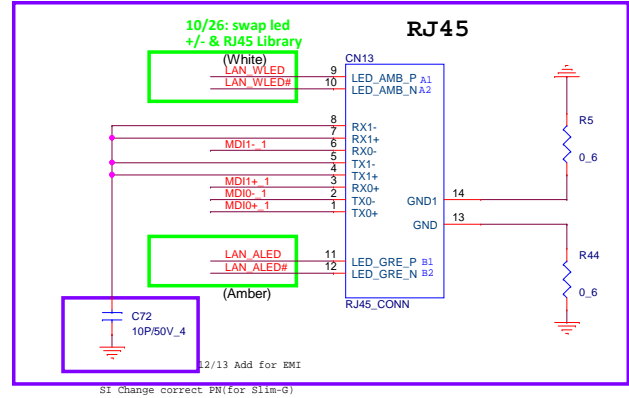


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

LAN conn

10/26: swap led +/- & RJ45 Library

RJ45

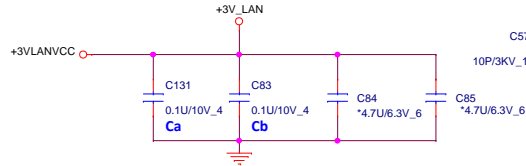


12/13 Add for EMI

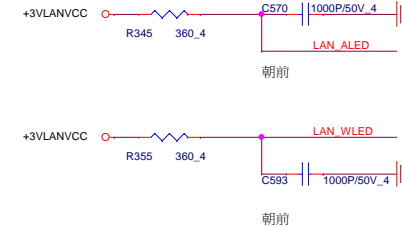
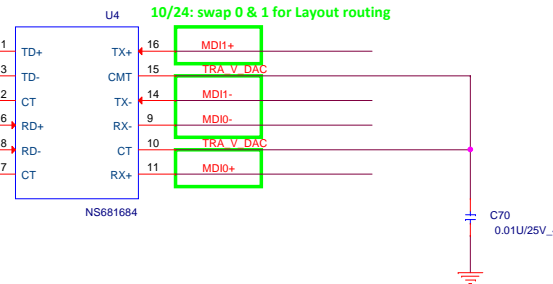
SI change correct PN(for Slim-G)

For 10/100

Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32

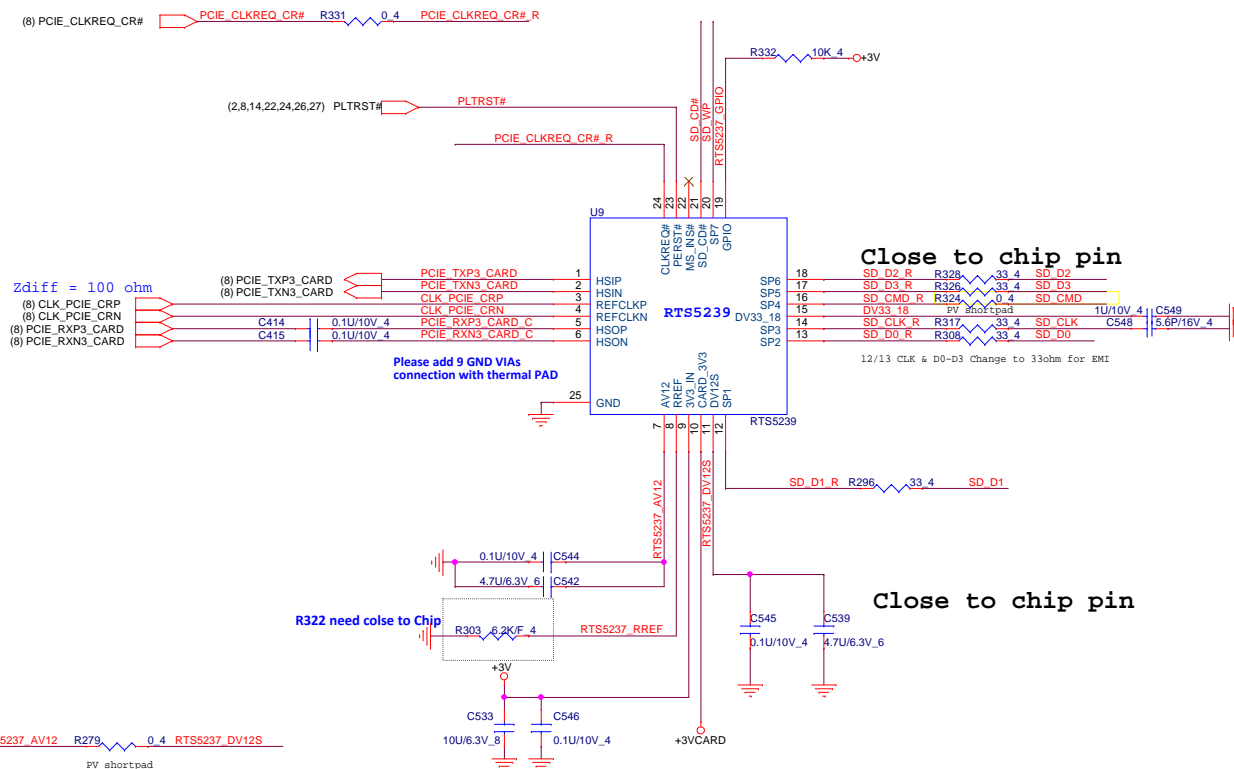


10/24: swap 0 & 1 for Layout routing



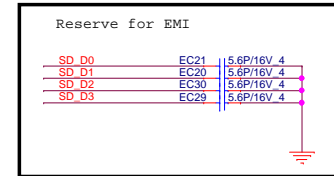
PROJECT :U81
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8166EH /RJ45 conn	1A
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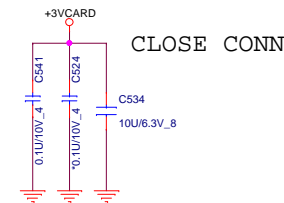
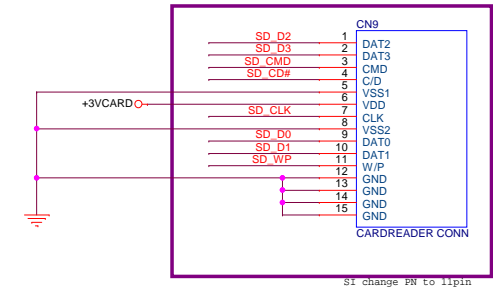


SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin



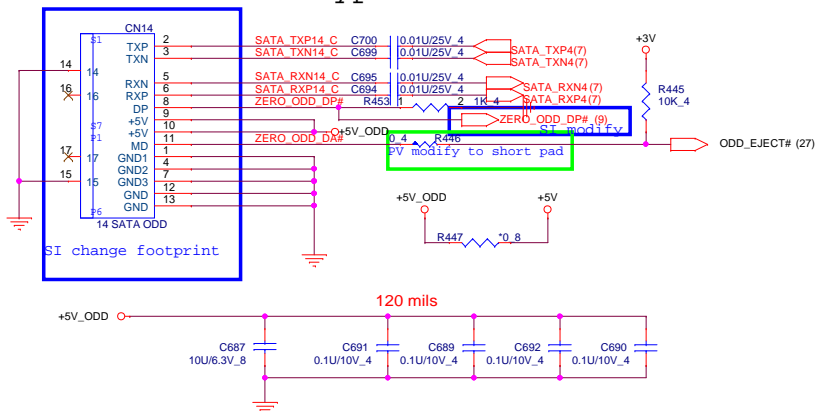
SD / MMC
CARD READER



SATA ODD CONNECTOR

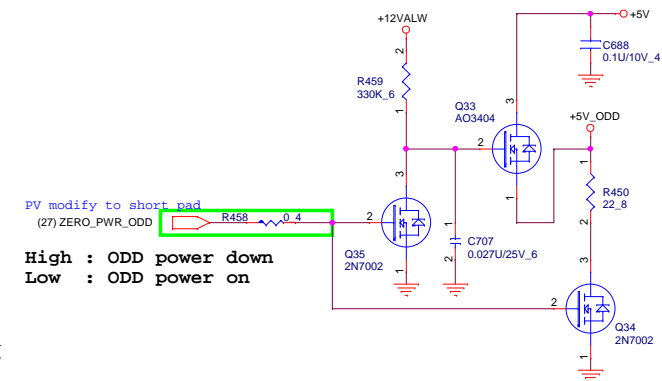
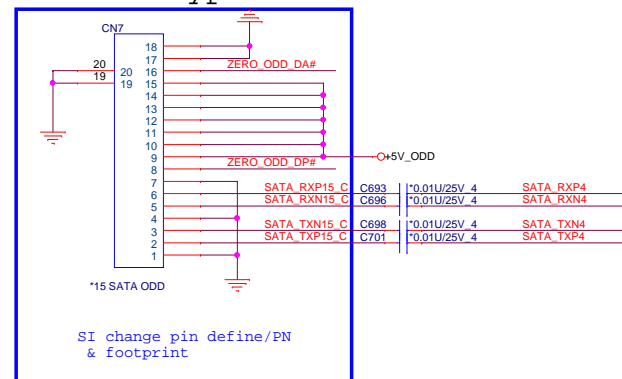
14" SATA ODD

Bypass CAP close conn



15" SATA ODD

New Type



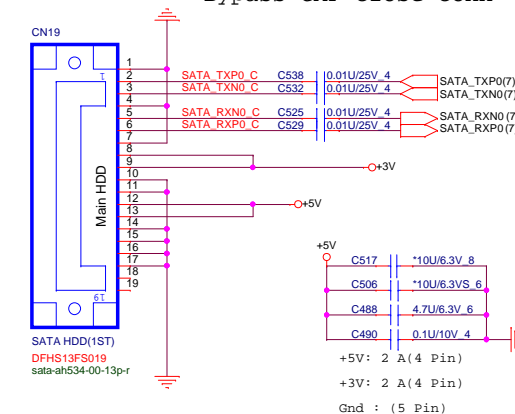
PROJECT :U81
Quanta Computer Inc.

Size Custom	Document Number CR RTS5239 & CR SOCKET	Rev 1A
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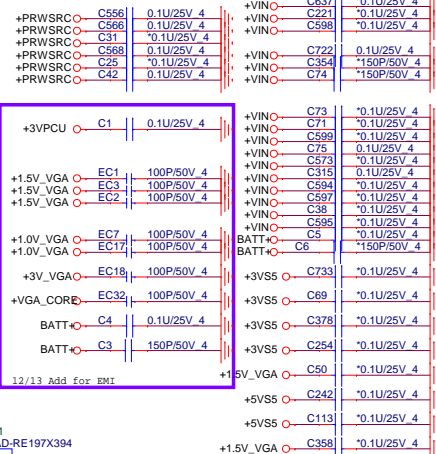
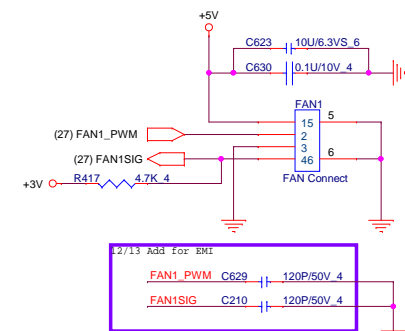
Hole



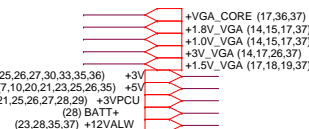
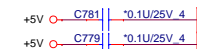
Bypass CAP close conn



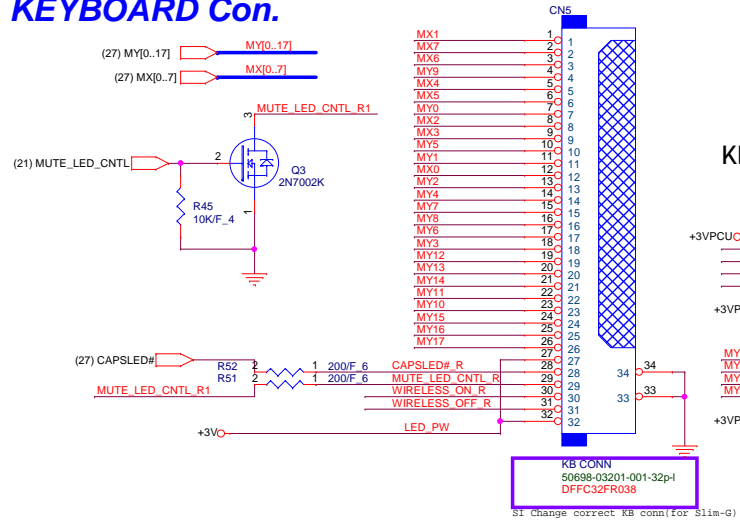
FAN



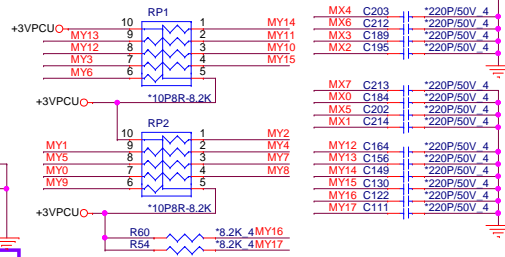
Mini PCI-E Card 2- Full size mSATA



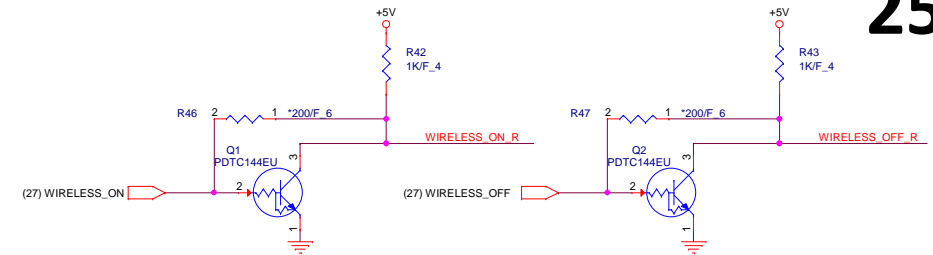
KEYBOARD Con.



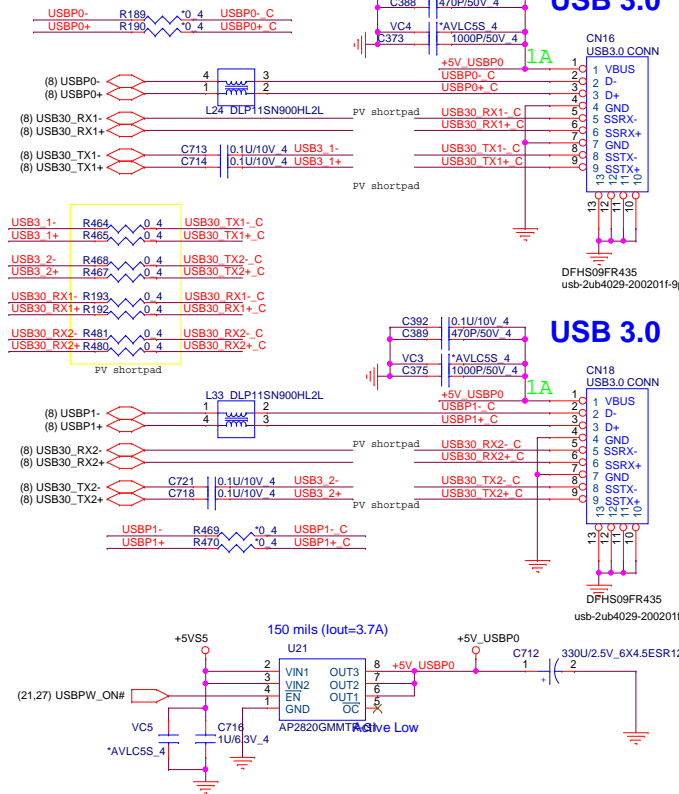
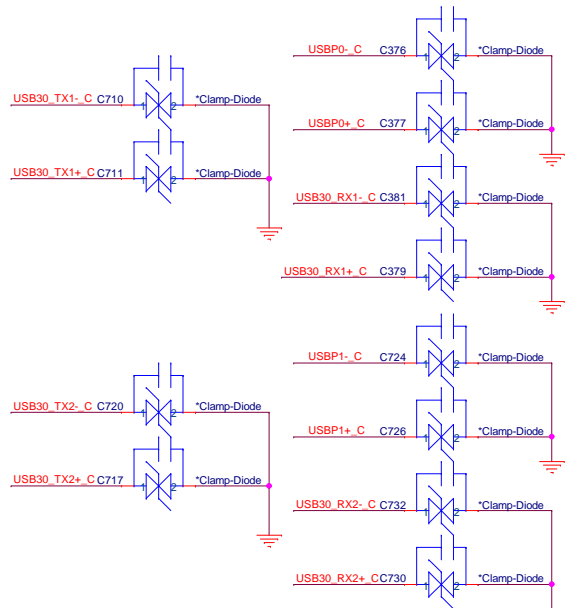
KEYBOARD PULL-UP



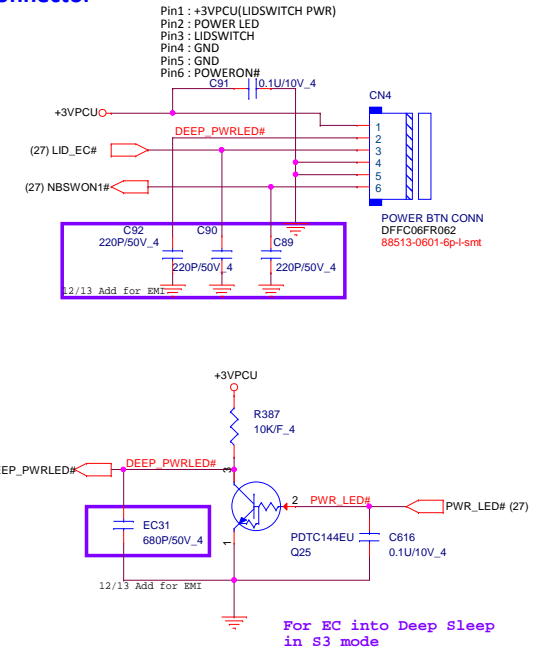
25



USB 2.0/3.0 Combo

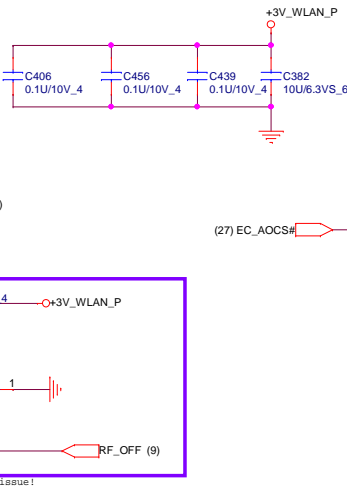


Power Button Connector



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Quanta Computer Inc.		
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Custom	USB 3.0/KB	1A
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+3V_WLAN_P	SI change for DS3 leakage issue!
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Accelerometer Sensor

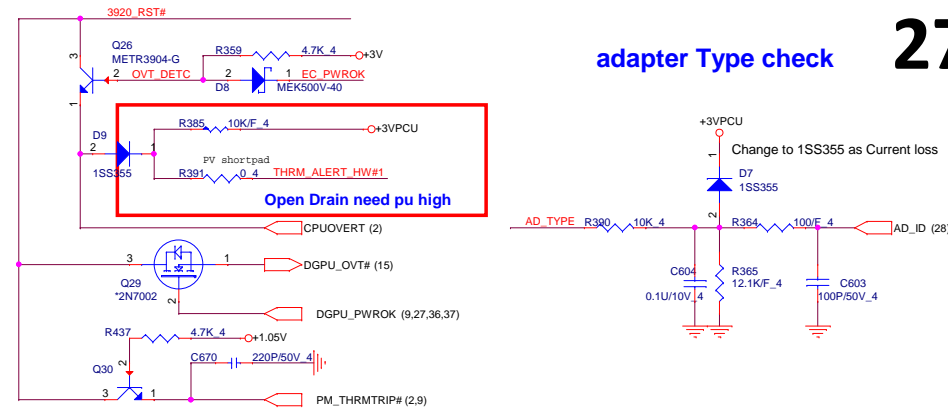
Touch screen



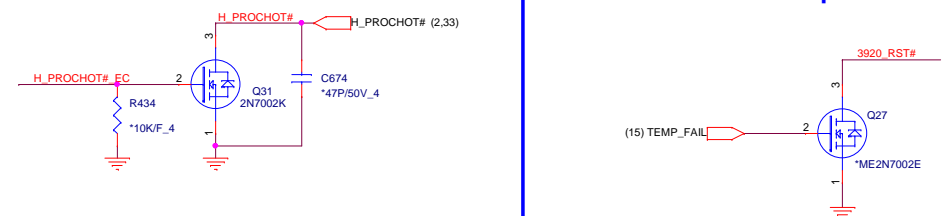
Green CLK Circuitry



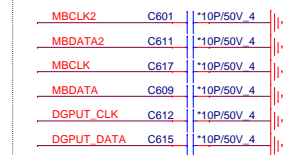
adapter Type check



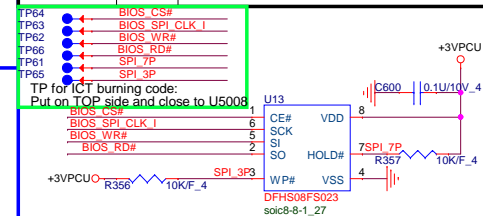
DGPU Thermal protect

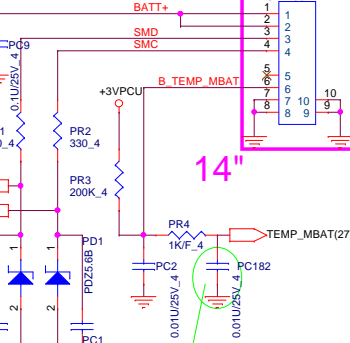


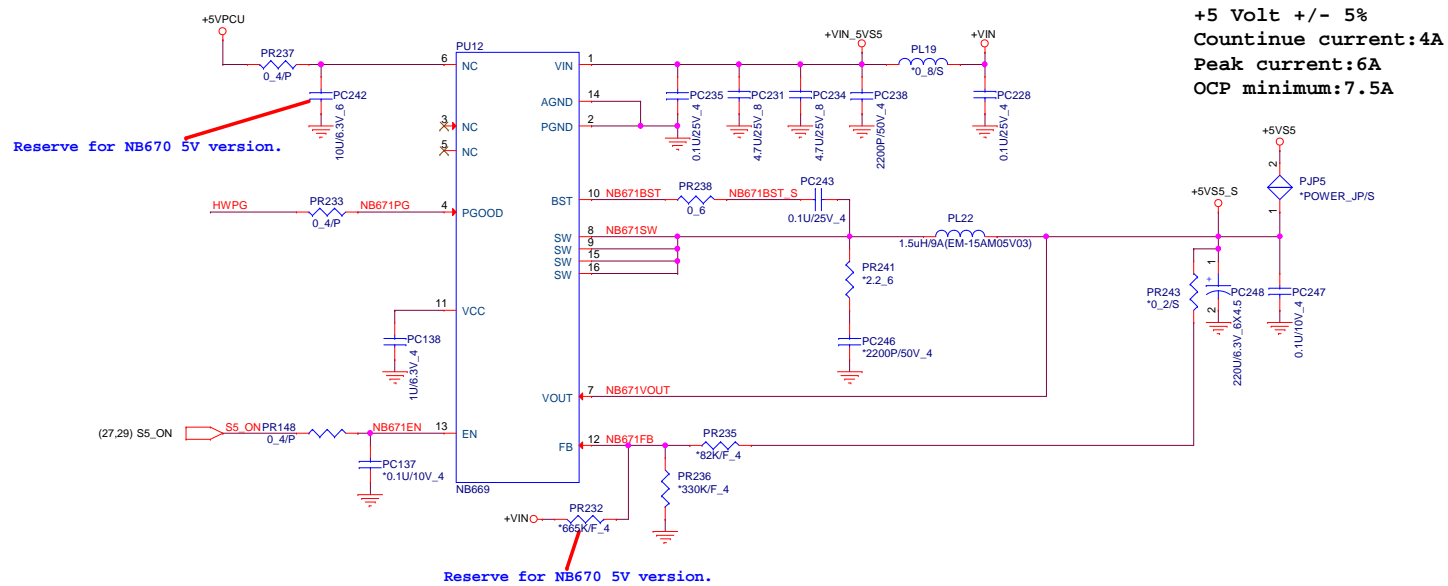
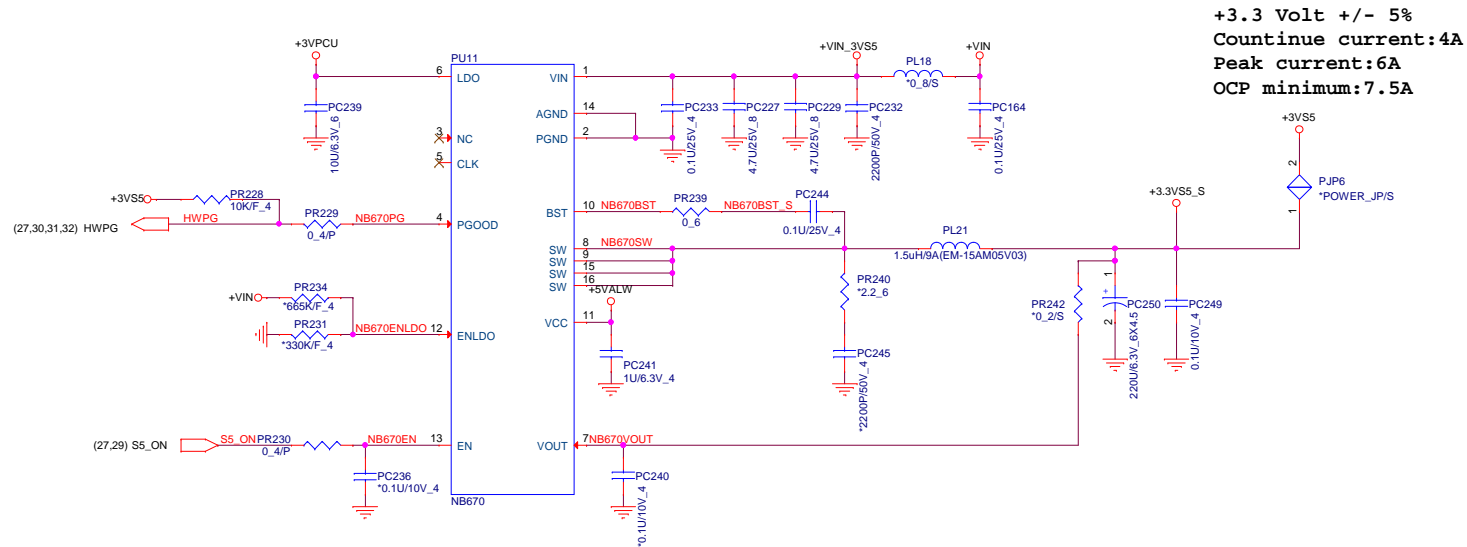
Reserve for ENE Hold time issue




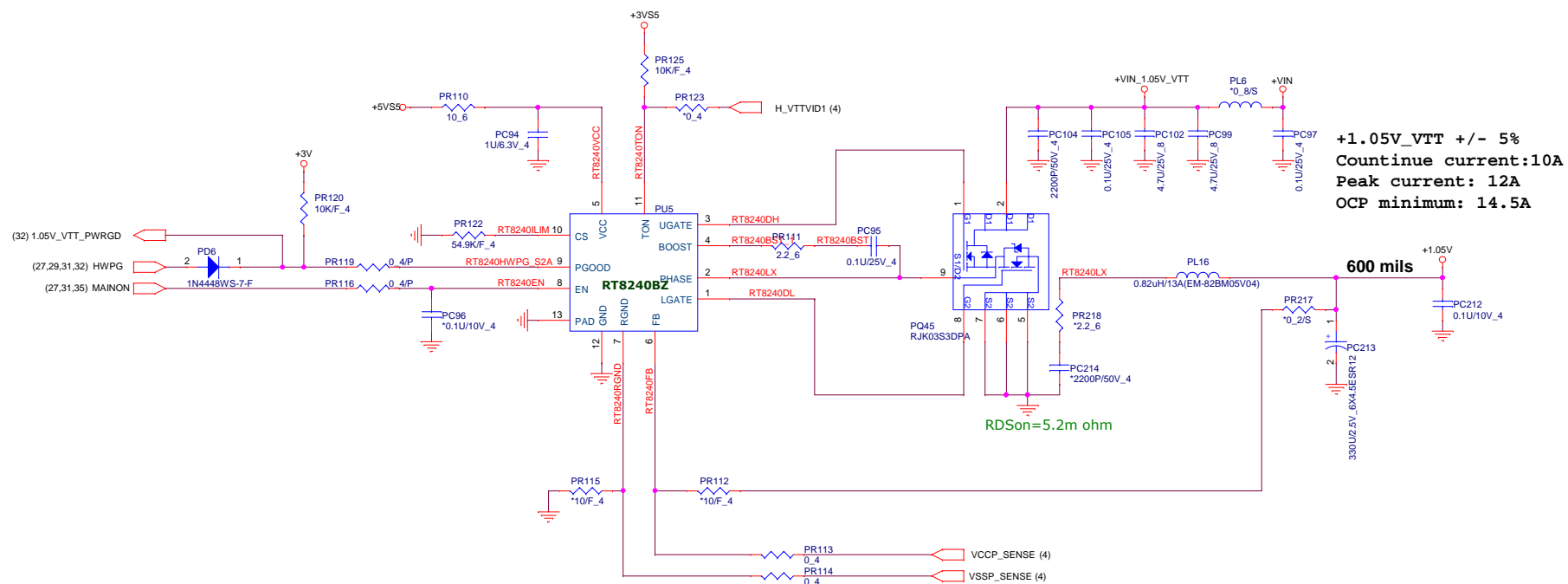
Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EON EN25Q80A-100HIP)
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023







 PROJECT :U81 Quanta Computer Inc.		
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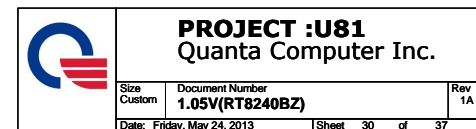


+1.05V_VTT +/- 5%
Continue current: 10A
Peak current: 12A
OCP minimum: 14.5A

600 mils

RD_{SON}=5.2m ohm

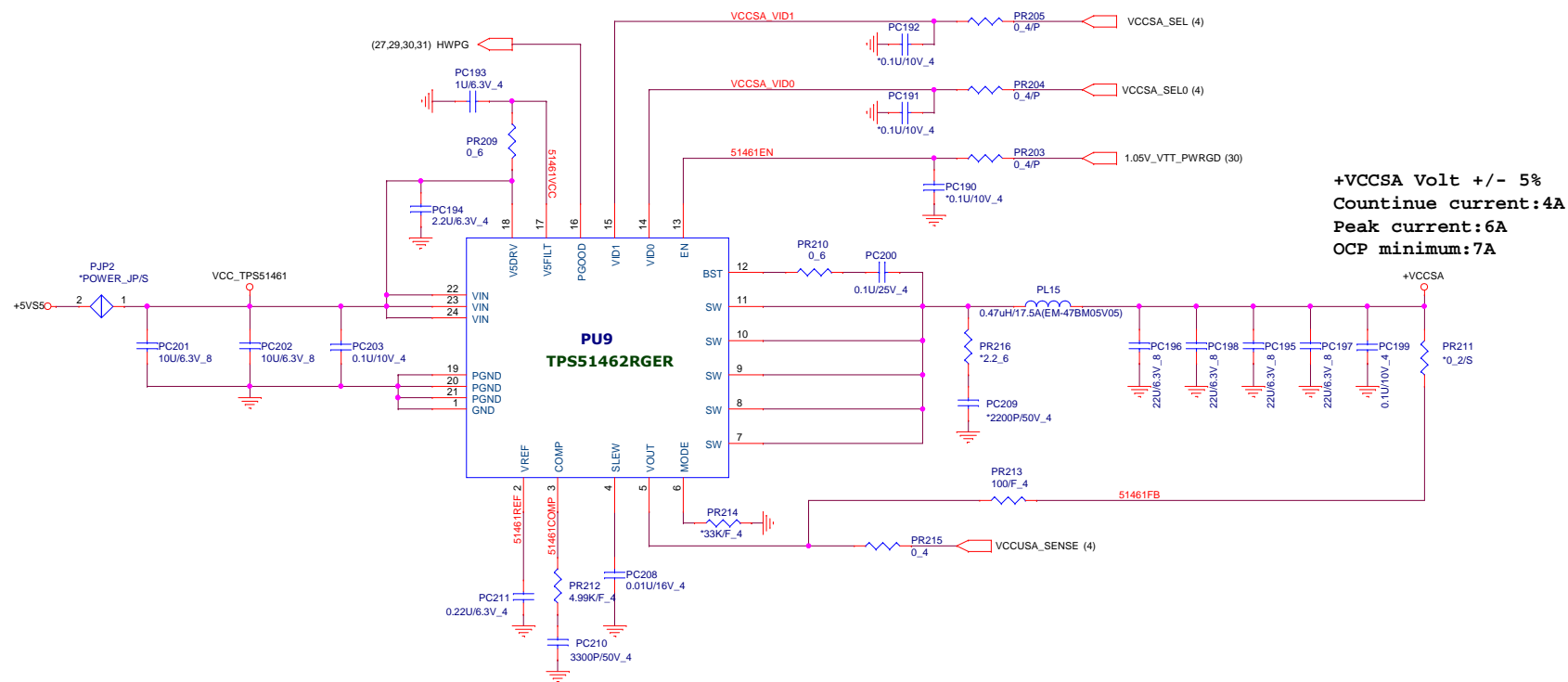
 +1.05V (2,4,6,7,8,10,26,27,33)

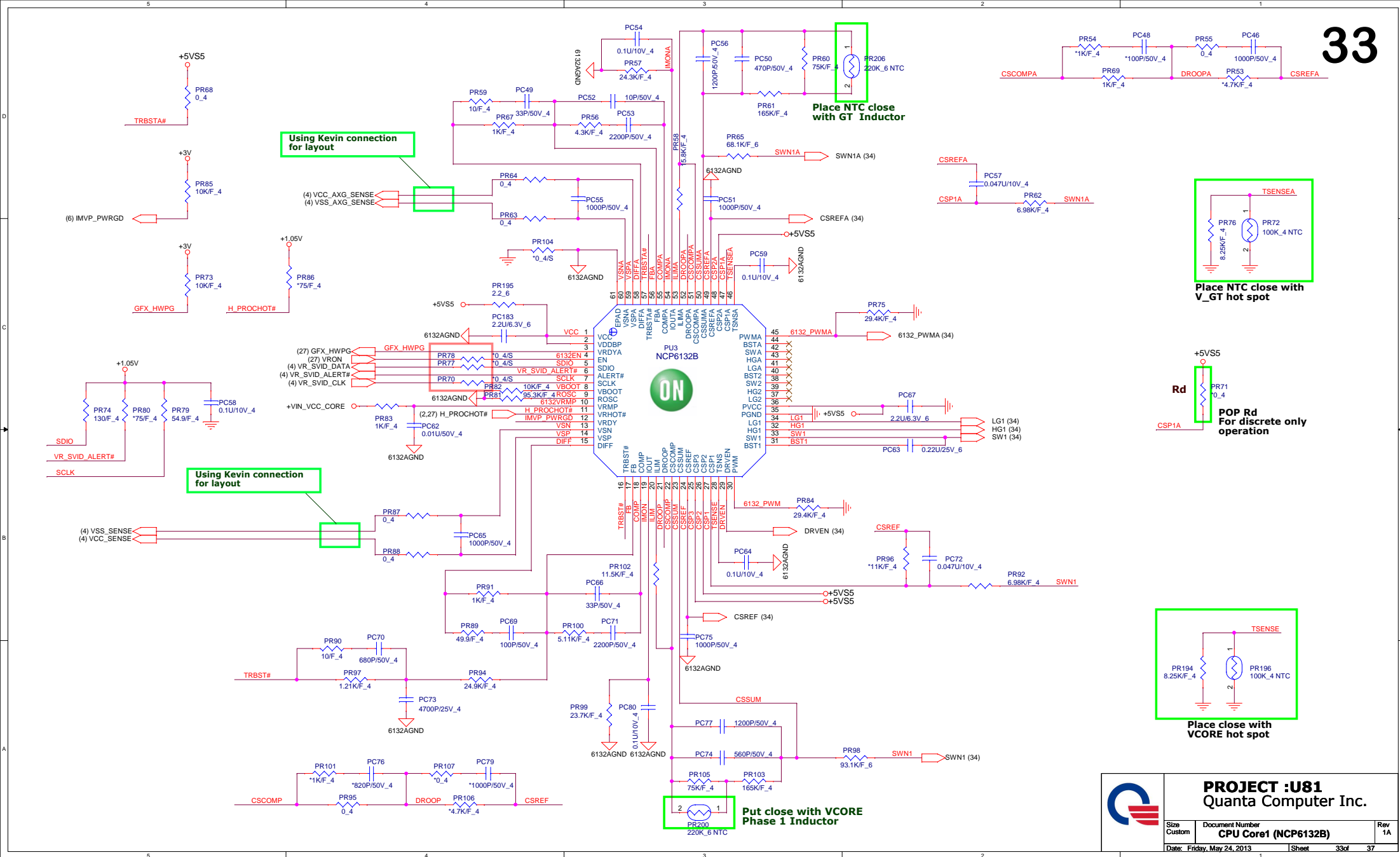


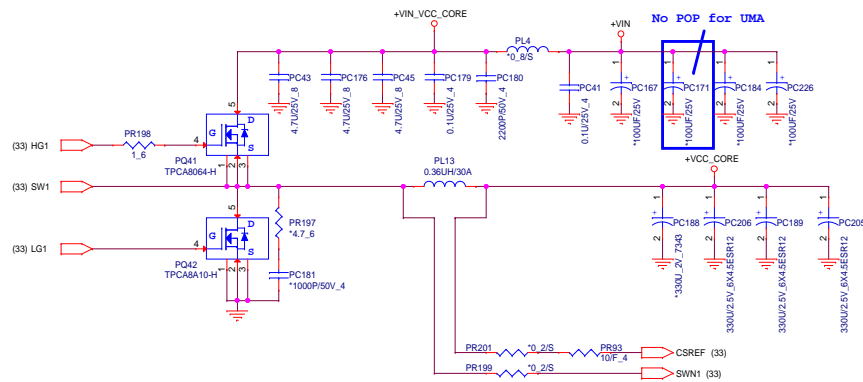
TPSS1462RGER/AL051462000

For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

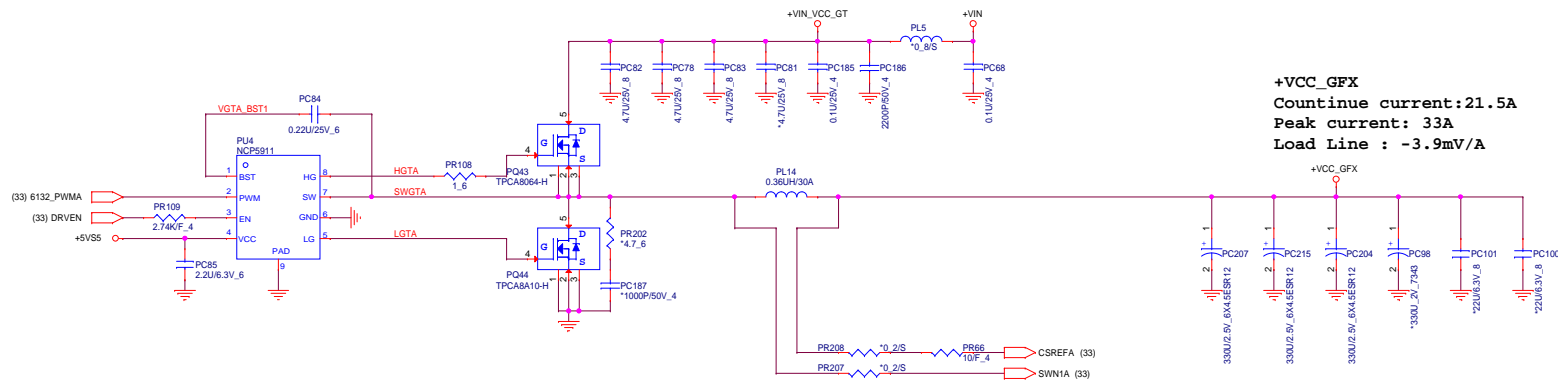
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



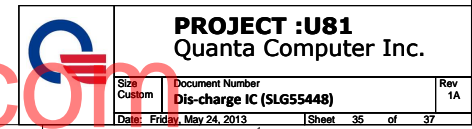




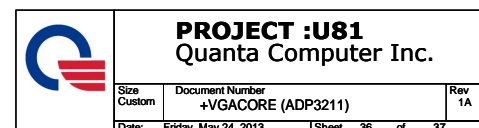
+VCC_CORE (ULV 17W)
 Countinue current:16A
 Peak current: 33A
 Load Line : -2.9mV/A



+VCC_GFX
 Countinue current:21.5A
 Peak current: 33A
 Load Line : -3.9mV/A



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VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A

